Avalanche-induced thermal instability in Ldmos transistors

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Abstract

Safe operating area limits for large Ldmos are shown to be due to a thermal instability mechanism initiated by avalanche generated carriers which turn-on the parasitic bipolar transistor. An analytic model is described and is shown to agree well with experimental data.

Introduction

This paper is concerned with the Safe Operating Area (SOA) of Ldmos transistors. Negative resistance, initiated by an electrical instability, has been identified as an important effect that can determine the SOA, [1]. "Electro-thermal" effects have also been studied in connection with limits on the current and voltage of the Ldmos, [2], [3]. A more detailed treatment, using device simulation, has also been presented in [4].

In this paper we describe a new analytic model of bipolar transistor thermal instability as it applies to the Ldmos. The model differs from previous bipolar models used to predict "FBSOA"[5]. In the new model, the base is not driven from its terminal, but is driven "internally." Avalanche-generated base current, emanating from the bird's beak impact ionization zone, becomes responsible for turning on the bipolar. When the self-heating due to this mechanism reaches a critical point, thermal instability ensues. Thermal instability can occur at relatively low values of V_{GS} and can give a "thermal" safe operating area that is well within the "electrical" SOA predicted by [1], an observation that has also been made in [4].

Fig. 1 describes the general features of the electrical and thermal SOA. The dashed lines indicate the shape of the thermal and electrical boundaries. The constant V_{GS} curve shows the onset of snapback, defining the electrical SOA boundary. The movement of the electrical SOA boundary with increasing temperature is indicated.

The thermal SOA boundary corresponds to the onset of thermal instability. A stability factor S can be defined as

$$S = V_{DS} \cdot Rth(t) \cdot \frac{\partial I_D}{\partial T} \Big|_{Vds,Vgs=const} \qquad (1)$$

where $S=1$ defines the point of thermal instability[5]. $Rth(t)$ is the time dependent thermal resistance and T is the temperature of the Ldmos "heat source" at the wafer surface.

Throughout most of the Ldmos operating range, the temperature coefficient of I_D is negative, giving a negative S, and a stable system, however, $\partial I_D/\partial T$ can become positive at high voltages where bipolar action becomes important. In this region, $S>1$ can occur.

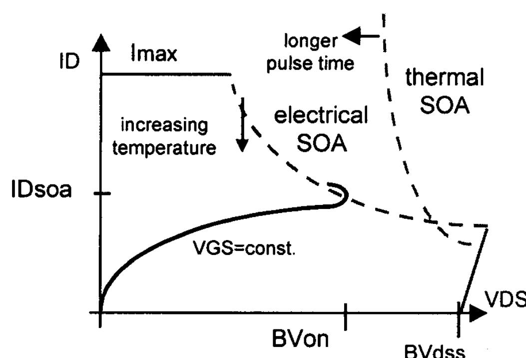

Fig. 1. Diagram showing boundaries that define the thermal and electrical safe operating areas.

Modeling heat flow

It is important to have good models of heat flow for calculating both the electrical and thermal SOA. We follow the Green's function approach of [2], where the heat source is assumed to be a thin rectangle of dimensions $a \times b$ on a semi-infinite chip surface at $z=0$. A three-dimensional view of the heat flow region is shown in Fig. 2. One quarter of the Ldmos heat source region is indicated by the patterned rectangle on the surface. The temperature at a point x,y,z in response to a step of power P is given by

$$T(x,y,z,t) = \frac{P}{4 \cdot a \cdot b \cdot K\theta \cdot \sqrt{\pi}} \cdot \int_0^{2 \cdot L\theta(t)} \exp\left(\frac{-z^2}{u^2}\right) \cdot \left[erf\left(\frac{a/2+x}{u}\right) + erf\left(\frac{a/2-x}{u}\right)\right] \cdot \left[erf\left(\frac{b/2+y}{u}\right) + erf\left(\frac{b/2-y}{u}\right)\right] \cdot du \qquad (2)$$

where u is the integration variable and has dimensions of length. $K\theta$ is the thermal conductivity and $L\theta(t)$ is the thermal diffusion length, defined by

$$L\theta = \sqrt{D\theta \cdot t} \qquad (3)$$

where $D\theta$ is the thermal diffusivity. For use in (1), the thermal resistance is defined as the ratio of $T(0,0,0,t)/P$ and can be written as

$$Rth(t) = \frac{1}{a \cdot b \cdot K\theta \cdot \sqrt{\pi}} \cdot \int_0^{2 \cdot L\theta(t)} erf\left(\frac{a/2}{u}\right) \cdot erf\left(\frac{b/2}{u}\right) \cdot du \qquad (4)$$

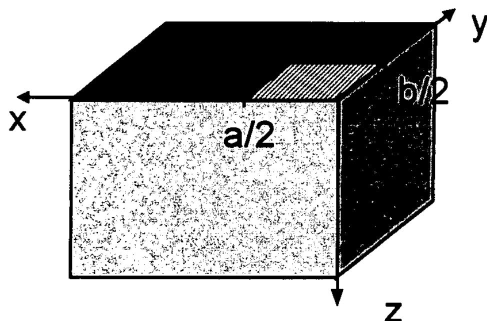

Fig.2. Three-D view of semi-infinite silicon slab with a rectangular heat source of dimensions $a \times b$ representing the Ldmos.

If the heat source extends beyond the surface significantly, a "volume" or three-dimensional heat source solution should be used [6].

Thermal resistance for the case of a square heat source is plotted vs. heat source area $A=a^2$ and pulse time t in Fig. 3. $K\theta$ is 1 W/K-cm and $D\theta$=0.5 cm2/s. (These values are used throughout the paper.) This plot demonstrates a number of important effects that occur as pulse time and heat source area change.

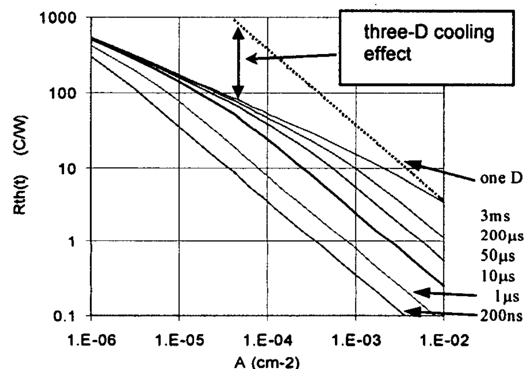

Fig. 3. Time dependent thermal resistance vs. heat source size for different pulse times. Heat source is a square. The one-D plot is for a thickness of 375 μm.

For short pulse times, heat flow is nearly one-dimensional and flows vertically from the source. In this case, $Rth(t)$ is proportional to $1/A$. For long times, and small A, $Rth(t)$ becomes proportional to 1/sqrt(A), corresponding to radial heat flow, however, as A increases, there will be a change to $1/A$ proportionality. All these behaviors are important when it comes to determining Ldmos SOA

For small devices, and with t greater than about 50 μs, radial heat flow provides a three-D "cooling" effect which limits the temperature rise. This means that electrical effects, as noted in [1], are likely to determine the SOA. As Ldmos size increases, three-D cooling becomes less effective, and the heat removal process can degrade to the point where thermal instability needs to be considered.

It is true that thermal instability effects can be taken into account using finite-element, electro-thermal simulators, however, for large structures, an excessive number of nodes may be required, limiting use in device designs. The simulation approach is explored further at the end of the paper.

Electrical SOA and evidence for thermal instability

Fig. 4 shows a plot of snapback current normalized to gate width W vs. device size for a 60V Ldmos similar to the design described in [7]. The Ldmos gate includes a polysilicon field plate over field oxide that provides the high voltage blocking capability. Source-drain half pitch is 7.2μm. In Fig. 4, the solid line shows $IDsoa/W$ values computed using isothermal simulations, following the method described in [1]. The temperature is determined via a self-consistent approach, using $Rth(t)$ from (4) with t=3ms. The decrease in $IDsoa/W$ that occurs as T increases can be ascribed primarily to the temperature dependence of electron saturation velocity.

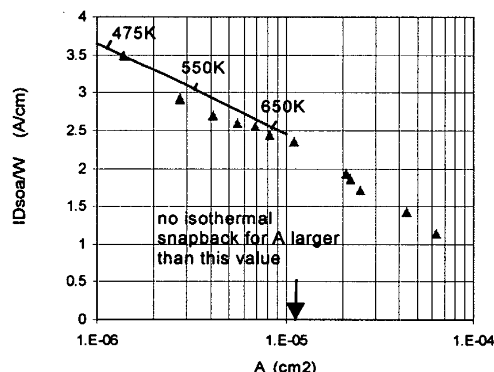

Fig. 4. Snapback current per unit gate width vs. device size. Solid curve shows isothermal simulation results. Points are curve tracer measurements on different W Ldmos all having same SD cross-section. VDS=50V.

Above a temperature in the range 700 to 750K, the isothermal simulations of Fig. 4 show no electrical snapback. The reason for this result is that multiplication M and bipolar gain α are functions of T. Eventually a temperature is reached where it is no longer possible to achieve the snapback point $M{\cdot}\alpha$=1 and the device remains electrically stable.

Nevertheless, it is clear from Fig. 4 that devices are failing as A, and therefore T, are increased. For this reason, we need to question the isothermal assumption and the application of the electrical snapback model to large Ldmos.

As further evidence that two different mechanisms are responsible for snapback, Fig. 5 shows two curve tracer photos where the Ldmos is operating just below the point of failure. The upper photo is for a "small" device. In this

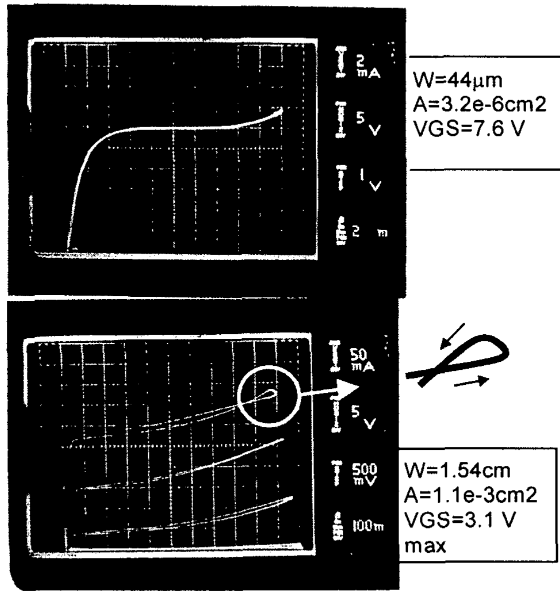

Fig. 5. (upper), I_D vs. V_{DS} for constant V_{GS}. No loop is visible prior to snapback. (lower), 6 V_{GS} steps at 0.5V/step plus 0.1V AID. Loop is visible at 50V, 380mA.

case, no loops are seen. A much larger device with the same cross-section is shown in the lower photo. For the large device, a distinct "reverse" loop occurs as V_{GS} is increased. The inverse loop is evidence that creation of an additional current component is underway.

Description of the model

Fig. 6 shows a cross-section of the Ldmos operating in a region where impact ionization is taking place at the body-Nwell junction. The primary carriers are electrons flowing in the channel. The magnitude of this component, I_S, is mainly determined by V_{GS}. As shown in Fig. 6, a secondary hole current, produced in response to the I_S primaries, flows through the "pinched-body" sheet resistance R_s and creates a voltage drop $vBE(x)$. This voltage leads to a emitter current density, $Jv(x)$, which is exponentially related to $vBE(x)$ via the bipolar equation for emitter current, assuming current gain α is near unity.

The emitter current density can be integrated to find the total emitter current I_E. It is I_E that exhibits the positive temperature coefficient that leads to thermal instability. That is, it is I_E that produces the loop shown in Fig. 5

An approximation for the multiplication factor $Mn(VGS, VDS)$ can be obtained by fitting Miller's equation to the measured data. The relevant equations are shown in Fig. 7. Eqs. (5) through (10) are solved by fixing V_{DS} and varying V_{GS}, giving I_D, T, Mn, S, and $vBE(0)$ as outputs. A spreadsheet is a useful way to implement the procedure. Fig. 8 shows an example of this approach where A =1e-3 cm2, which is to the right of the isothermal

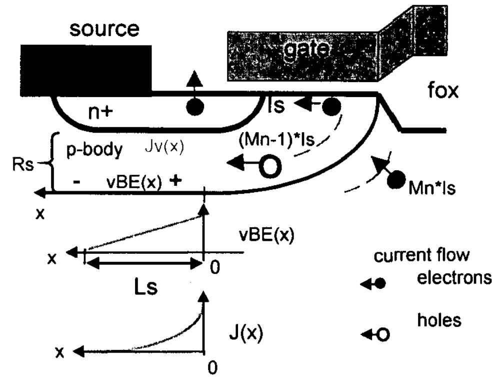

Fig. 6. Cross-section showing current components due to impact ionization. Mn accounts for avalanche multiplication. Avalanche generated base current turns on the bipolar, giving $Jv(x)$.

$$vBE(0) = \frac{Ls}{W} \cdot Rs(T) \cdot IS0(T) \cdot (Mn - 1) \qquad (5)$$

$$I_E = W \cdot \frac{q \cdot ni^2}{GB} Ls \cdot \frac{kT}{q \cdot vBE(0)} \cdot \left[\exp(\frac{q \cdot vBE(0)}{kT}) - 1 \right] \qquad (6)$$

$$S = V_{DS} \cdot Rth(t) \cdot \frac{\partial I_D}{\partial T} \qquad (7)$$

$$I_D = Mn \cdot (I_S + I_E) \qquad (8)$$

$$Mn = 1/[1 - (\frac{V_{DS}}{BVdss})^{mx(V_{GS})}] \qquad (9)$$

$$T = I_D \cdot V_{DS} \cdot Rth(t) + TA \qquad (10)$$

Fig. 7. Equations for base-emitter voltage, emitter current, stability factor, total drain current, multiplication factor and temperature $IS0$ is the low voltage drain current. GB is the base Gummel number. $mx(V_{GS})$ is obtained by fitting Miller's equation to the drain characteristic.

limit indicated in Fig.4. The line S=1 gives the desired solution. The temperature at the instability point is 560K, which is well below the electrical SOA temperatures shown in Fig. 4. It can be seen that S=1 corresponds to an emitter current that is only a few percent of the total drain current. From Fig.5, the loop "size" is about 2 mA , or about 5 percent of the total I_D. Based on this comparison, we can say that Fig. 8 is consistent with the idea that the loop is primarily due to bipolar emitter current.

Fig. 9 shows the results of applying the instability model to different size Ldmos for two pulse times, 3ms and 300μs. The 3ms model results agree well with measurements, however, for the 300μs pulse time, the model predicts smaller I_D/W vs. measured data, with an error of about a factor of two. One possibility for this discrepancy is that the Ldmos of Fig. 9 uses topside copper metallization, which is similar to the structures reported in[4], and [8]. For 300 μs, the thermal diffusion length in Cu is about 17μm, which is close to the Cu

thickness. For longer times, e.g. 3ms, the diffusion length grows and the topside heat flow benefit diminishes.

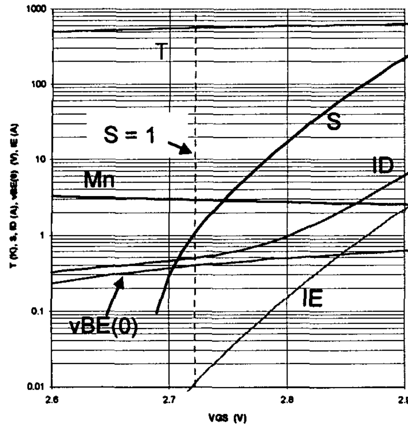

Fig. 8. An example of the model results, plotting temperature, stability factor, drain current, multiplication factor, base-emitter voltage at x=0, and emitter current vs. gate-source voltage. t=3ms, Ls=2.5µm, Rs=3kohm/sq, A=1e-3 cm2, V_{DS}=50V, $BVdss$=70V.

Electro-thermal simulations

If we consider the case where heat flow is nearly one-dimensional, electro-thermal simulations become of interest. The usual method of constructing a two-D cross-section of the source-drain region can be used, making sure there is a certain thickness of silicon, *zeff*, from the top surface to a bottom "thermal contact," which is typically set to 300K. The main question is how to determine *zeff*.

We have used the equation for temperature, (2), to determine a value for *zeff* by extrapolating the near-linear temperature profile at the surface to a distance where the temperature rise is zero, that is, the thermal contact. An example for *zeff* = 150 µm is shown in Fig. 10. For the simulation, V_{GS} is set to 1.8V and V_{DS} is a step of 50V. After about 4.5ms, the drain current increases rapidly, indicating the onset of instability. The temperature response is also shown in Fig. 10. Initially T starts out as sqrt(t) dependent, however, at 3.7 ms, an inflection point is seen and I_D develops a positive temperature coefficient and finally increases rapidly at 4.5 ms.

Conclusions

A relatively simple analytic model has been described which shows how large Ldmos can become thermally unstable under conditions that frequently exist in IC output driver stages. Good agreement with measurements has been demonstrated. The model can be used to make SOA estimates of initial Ldmos designs. A method for adapting the thermal analysis to calculate an effective silicon thickness for electro-thermal simulations has also been proposed.

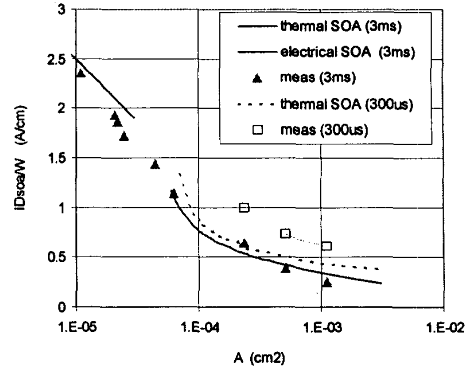

Fig. 9. Drain current per unit gate width vs. device size, showing isothermal and thermal instability model predictions. Measurements are for 3ms and 300µs.

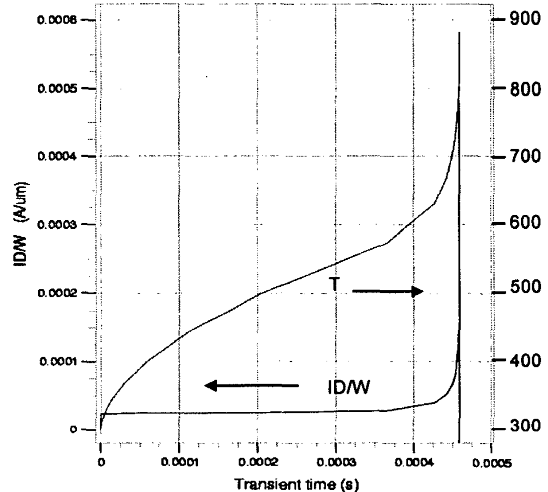

Fig. 10. Drain current per unit gate width and Ldmos surface temperature vs. time for an electro-thermal simulation with *zeff*=150mm.

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