Electro-Thermal instability in low voltage Power MOS:Experimental characterization.

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Abstract – **In this paper we will present experimental results of dynamic thermal mapping on a new class of low voltage high current power MOS. The reported results underline that, as in the case of power BJTs, also in this class of devices the hot-spot phenomenon occurs. Moreover, here we give a theoretical interpretation of this phenomenon and propose a novel approach to understand the causes that can determine the temperature instabilities in such kind of MOS devices.**

I. Introduction.

It is well known that in the case of power BJTs, the device electro-thermal instability is one of the main causes for the reduction of the Forward Bias Safe Operating Area (FBSOA); this phenomenon is due to the positive temperature coefficient of the collector current in a wide range of currents [1,2].

Up to now, this kind of thermal limitation on FBSOA has not been observed in power MOS devices, because they generally present a negative temperature coefficient of the drain current. However, recently, in a new class of low voltage & high current power MOS, a significant reduction of the forward bias SOA reduction has been observed, similar to what happens in BJT's.

In this paper, we will prove that, as in the case of BJTs devices, the observed reduction in forward bias SOA of Power MOS, is due to a temperature instability mechanism induced by an uneven distribution in drain currents in the chip.

In the following, we will present some experimental results for this phenomenon and will propose a novel numerical approach to understand the causes that can determine the electro-thermal instabilities in such kind of MOS devices.

The experimental techniques used to characterize electro-thermal instabilities in power devices usually present some limits [3]. In order to overcome such limitations, we have used a direct non-contact thermal mapping system [4]. Our set-up, below described, is based on a radiometric sensor, allowing both dynamic and steady-state thermal mapping, with high spatial resolution (less than 10μm), high time resolution (less than 10μs), and quite good temperature resolution (less than 0.5°C).

II. The Measurement Set Up.

As the sensor to detect the dynamic temperature, we use a radiometric microscope with a single cooled InSb sensor working in the range of wavelength from 2.5μm to 5μm (first Infra Red window). The microscope optic system has an equivalent spot size of about 8μm with a working distance of 2.5mm. The 2D scanning of the mapped surface is achieved by means of a x-y step motor stage controlled via IEEE-488 bus by a PC. As a matter of fact, the DUT is shifted respect to the microscope spot in order to cover all the surface under observation. By considering both the microscope spot size and stepping accuracy, we can allow spatial resolution less than 10μm over an extended area of 50×50 mm^2. Step by step, the radiometric waveforms, coming from the InSb sensor, are acquired by means of a digital oscilloscope, controlled via the IEEE-488 bus, too. The oscilloscope also performs the pre-filtering of the detected signal by using an averaging procedure to increase the signal to noise ratio [5].

The measurement procedure for the dynamic thermal mapping is divided in phases described in the follow.

First of all, we define on the DUT surface an *acquisition grid* made of N points ($n_X \times m_Y$) where the radiometric waveforms will be acquired.

It is important to remember that the radiometric systems are able to perform absolute thermal measurement only if the target emissivity coefficient is known. Unfortunately, the surface of power devices is often composed of different material (i.e. aluminum, passivation, silicon oxide, etc.) that are characterized by different emissivity coefficients. Hence, in our thermal mapping procedure, an outline step (the Emissivity Mapping: EM) is also performed in order to know the emissivity coefficients of the N points of the *acquisition grid.*

During dynamic measurement, the DUT is biased with a repetitive pulsed power bias; the maximum voltages and currents are usually chosen to bias the device at the limit of their pulse SOA. To prevent temperature pumping the bias time repetition is set long enough to achieve the complete dissipation of the generated heat between the following pulses (duty cycle less than 10%).

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After acquired all the N programmed waveforms, the numerical elaboration of the radiometric transient signals starts. First of all, the stored dynamic radiometric signals are appropriately corrected by using the emissivity coefficient of the relative point (measured during the EM) and converted in the true dynamic temperature signal. After, the $n_X \times m_Y$ arrays, are managed to obtain 100 2D-arrays that represent time frames of the temperature distribution on the DUT.

II. Experimental Results.

By means of the above described experimental set-up we have tested some different power MOSFETs. In particular, in this work we show the results obtained by a new low voltage power MOS, rated 60V and 60A, characterized by a short channel length (0.8μm).

This devices present an experimental SOA (under pulse operation) like the one reported on fig. 1(each dot of the Fig. 1 is due to a failure of a different device). As one can note, the maximum dissipated power is almost constant at the range of Drain-Source voltages (V_{DS}) less than 25V; while, by increasing the V_{DS} over 25V, the slope of the curve increases. This is a clear indicator that something in the failure mechanism is changed.

In fact, when the failure happen with constant power biasing conditions ($P_D=V_{DS}\times I_D$), this means that the average thermal resistance (R_θ) of the device is unchanged, according with:

$$P_D = \frac{T_{JMAX} - T_{case}}{R_\theta}. \quad (1)$$

Otherwise, if the failure do not happen along a constant power curve, by the constant case temperature (T_{case}), this means that R_θ is changed. This can be due to a different electro-thermal behavior of the DUT; in particular, R_θ increases if only a little area of the chip is much hotter than rest of the chip.

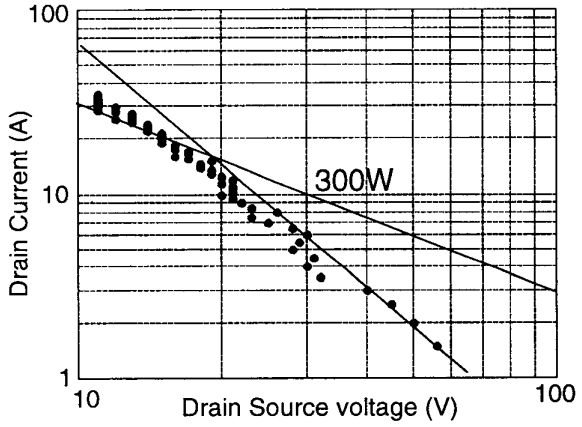
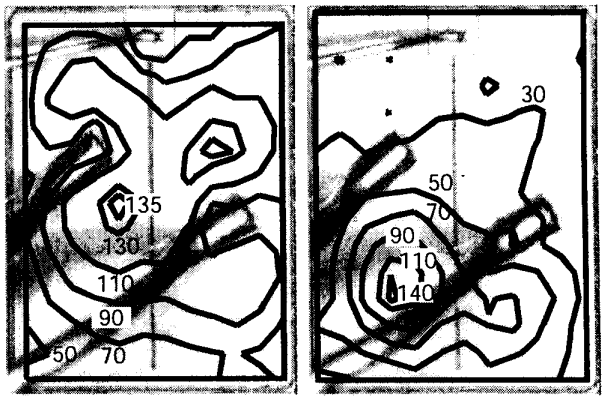


Fig. 1. Pulsed FBSOA of the tested MOS. Pulse length 100ms.



a) b)

Fig. 2. Temperature contour plots for the power MOS (the bounding wires and pads are shadowed) at bias conditions: a) V_{DS} = 15V, I_D = 18A; b) V_{DS} = 45V, I_D = 3.12A.

We have analyzed, by means of our non-destructive experimental system, the dynamic thermal distribution of the above described power MOS. One of the first interesting result can be obtained by comparing the thermal maps depicted in Fig. 2. Both maps are referred to the same MOS device at the end of the applied pulse (after 10ms),with two different biasing conditions, that give rise to an almost equal peak temperature: in the case of Fig. 2a, the bias was V_{DS}=15V and I_D=18A, in the case of Fig. 2b the biasing was V_{DS}=45V and I_D=3.12A.

It is evident, from these two thermal maps, in the case a) the temperature distribution is almost uniform on the whole device (the cold zones are referred to source and gate pads), while in case b) the main area of the device is cold and only a restricted area is very hot. This result prove that in these two different bias conditions the thermal dissipation of the device is not equivalent and give us the evidence that the R_θ parameter, in the two cases, is changed. To insure that this uneven thermal distribution is not present from the start of the power pulse we can see Fig. 3 and 4, where the transient temperature maps in the rang of 20°-140° are plotted.

In figure 3 there are reported four temperature maps at four time intervals during the application of the bias pulse, for the case V_{DS} = 15V, I_D = 16A; the pulse length was 10ms and the selected times were 1ms, 4ms, 7ms and 10ms.

It is evident, that with these considered bias condition (low voltage high current), the DUT heating is quite uniform on the chip area (without considering the inactive zones: gate and source pads), and during the application of the bias we can see only an increasing of the temperature.

In figure 4 the same temperature maps are reported, but now at a bias pulse with V_{DS} = 45V, I_D = 3.2A. Differently from the previous case, the heating is not uniform. Moreover, while in the first two frames the temperature distribution is uniformly low, in the second two frames we see the starting and the grown of the hot spot. At the end of the pulse only a little area of the chip has a temperature over 100°C, with a peak of about 140°C.

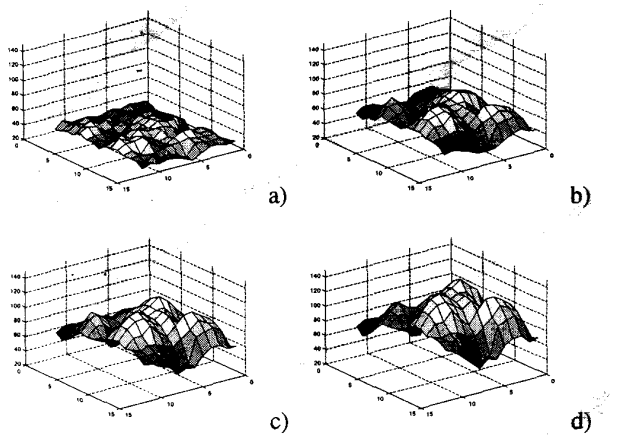


Fig. 3. DUT temperature maps at a) 1ms, b) 4ms, c) 7ms and d) 10ms for a bias equal to V_{DS}=15V I_D=16A.

A further proof that the thermal behavior is completely different in the two bias conditions can be done by plotting the transient of the hottest point on the DUT.

In figure 5, the dynamic behavior of the hottest point on the DUT in the first 30ms are compared for the two cases of 20V & 15A (curve A) and 40V & 3.5A (curve B). In both cases the temperature reaches over 160°C; but, while in the case A we can see a single time transient, in the case B the temperature behavior is firstly dominated by a single time constant, but afterwards it is exponentially increasing. The last behavior is the most dangerous for the safe of the DUT, in fact a small increase in pulse time length determines a very hard increasing of the maximum temperature, which can fail the device.

The two different dynamics are due to the different electro-thermal behavior of the DUT. In particular, in the case of the hot spot, when the instability starts, only a little area of the

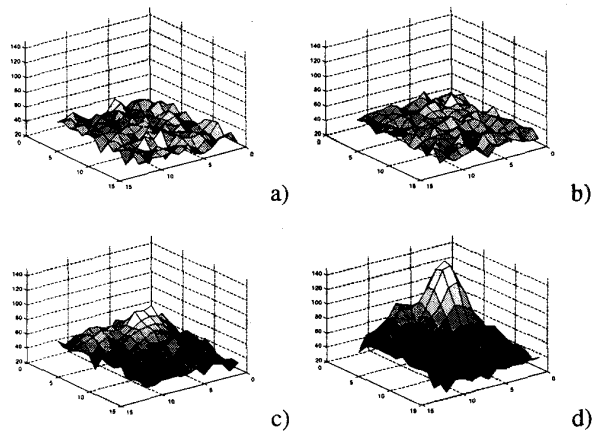


Fig. 4. DUT temperature maps at a) 1ms, b) 4ms, c) 7ms and d) 10ms for a bias equal to V_{DS}=45V I_D=3.2A.

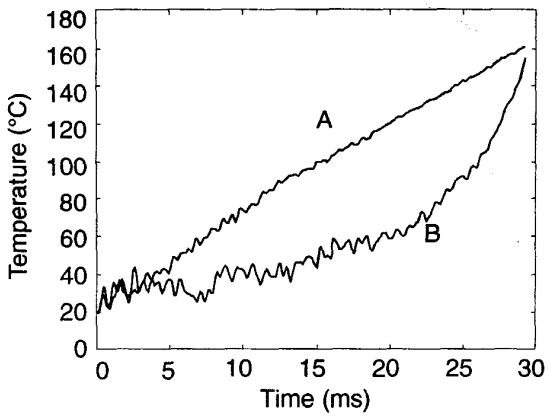


Fig. 5. Dynamic temperature of the hottest point on the DUT. A) V_{DS} = 20V; I_D = 15A. B) V_{DS} = 40V; I_D = 3.5A.

device increases the drain current density. This fact determines that only for this little zone the temperature is growing, and the increasing of the temperature, as be explained in next section, determines an increasing in the local drain current, which sustain and feed the temperature growing. This phenomenon is much more sensible in the low current range. In fact, the lower is the drain current, the higher is the current dependence from the temperature.

Finally, we report in Fig. 6, an *equivalent pulse SOA* obtained, differently to Fig. 1, without any MOS failure. The points depicted in such figure were obtained by biasing the device with different V_{DS}-I_D 10ms pulses. For all the reported biasing conditions, by means of our radiometer set-up, we observed the same final temperature value of the hottest point on the DUT (about 140°C). As shown in Fig. 6, we can see that, in order to observe equal maximum temperature peak on the device surface, we need to decrease the electrical power after a V_{DS} value of about 25V. This indicates that the thermal distribution, for the voltages above this value, become more uneven and unstable (as reported in Fig. 5). In fact, as it will discuss in next section, this kind of device has is a significant range of low level drain currents that show positive temperature coefficient, mainly due to the temperature coefficient of the threshold voltage and due to the high transconductance value. The SOA slope changes at a voltage higher than in the case of Fig. 1, because of the reduction of the pulse time length and the applied electrical power with respect to the case of Fig. 1.

III. Disussion and Conclusions.

In this section we give the electro-thermal model of a MOS, in order to underline the mechanism that give rise to the electro-themal instabiliy in a hig current device.

As we know [2], in the case of bipolar transistors, the hot-spot phenomenon occurs when the device presents a range of current where the temperature coefficient is positive. So, due to on a not equally distributed power dissipation on the chip,

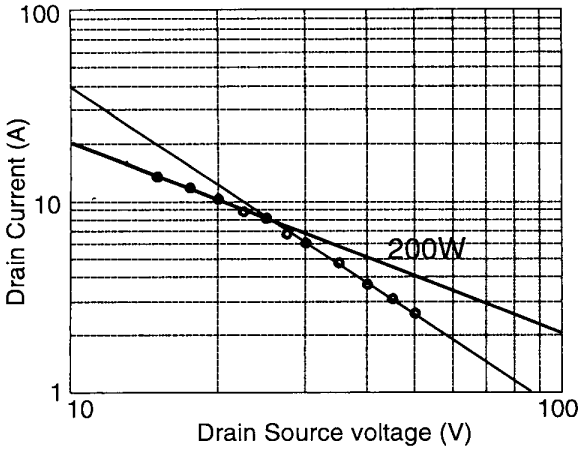


Fig. 6 Equivalent SOA of the DUT. In all bias conditions the hottest point reaches about 140°.

the termal runaway starts and it determines the growing of the hot spot.

Up to now, classical power MOSs show positive temperature coefficient only at very low drain currents; but nowadays, by increasing the device transconductance values (K), by reducing the channel length, the current range in which the temperature coefficient is positive is larger than before. In addiction, this kind of high current devices needs very low ON resistance (R_{ON}), obtained by increasing the epilayer doping. Also the low R_{ON}, mainly due to the resistance of the drift region, helps the electro thermal instability.

These design parameters can be kept into account in a simple electro-thermal numerical model of the MOS.

We can describe the MOS current I_D in the triode region, by considering the R_{Drift} (the resistance of the drift region), by means of:

$$I_D(T) = K(T)(2(V_{GS} - V_{th}(T))V_{DS} - V_{DS}^2). \quad (2)$$

where the active drain source voltage V_{DS} is dependent on the R_{Drift} and on the external applied V^*_{DS} by $V_{DS}(T) = V^*_{DS} - I_D(T)R_{Drift}(T)$.

Taking into account the active (V_{DS}) drain source value, we obtain a quadratic function of the quantity I_D, which solution is a non linear function of all the termines described above.

Moreover, when the device works in pinch off conditions, we consider the saturation of the drain current corrected by both the voltage drop due to the R_{Drift} and the channel length reduction.

In power MOSs, we know that the temperature coefficient of the threshold voltage ($V_t(T)$) is negative [7]. We have experimentally measured, in the case of the tested MOS, a V_t temperature coefficient of about -6.6mV/°C. Taking into account the temperature dependence of $R_{Drift}(T)$ and K(T) [7], we obtain the thermal dependence of the drain current as plotted in Fig. 7.

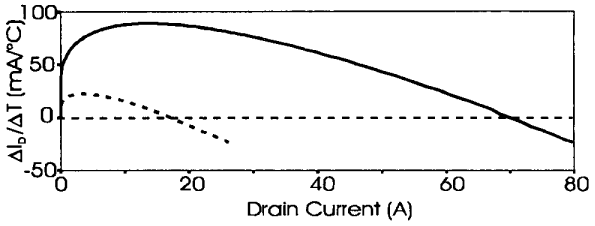


Fig. 7 Temperature dependence of the drain current vs. drain current for two different MOSFETs: Tested device K=29,6 A/V^2, R_{Drift}=18mΩ (continuos line); high voltage MOS K=6A/V^2, R_{Drift}=90mΩ (dashed line).

In figure 7 the thermal dependence of the drain current plotted versus the I_D at 27° of two different power MOSs: the tested device (continuos line) and a classical power MOS (dashed line) are compared.

As we can note, the tested MOS shows a much longer range where the temperature coefficient is positive and an higher maximum value, with respect to classical high voltage power MOS. In particular, the high value of K (obtained by using $L_{channel}$=0.8μm and equivalent $W_{channel}$=230cm), the low value of R_{Drift} (18mΩ at 27°C) and the high value of the temperature coefficient of threshold voltage play together to increase both the range and the maximum value.

This behavior produce a MOS device much more sensible to the hot spot phenomenon, especially when it is biased with low current and high voltages.

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