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Modeling the Onset of Thermal Instability in Low Voltage Power MOS: an Experimental Validation

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Abstract

The aim of this work is the validation of a recently proposed analytical model for the prediction of thermal instability in Power MOS by means of experimental evidence. The analysis of a number of commercially available devices illustrates the critical role played by some basic electrical parameters on the thermal ruggedness. In particular, it is shown that transistors with large threshold voltage values are more prone to thermally-induced limitations in pulsed Safe Operating Area (SOA).

I. INTRODUCTION

New-generation high-current, low-voltage vertical Power MOSFETs have been shown to exhibit positive temperature coefficient in a large range of Drain currents, which may give rise to thermal instability when the Drain voltage is increased and to consequent limitations in pulsed SOA [1], [2]. In [3] an analytical model has been presented for the onset of thermal instability, based on a few electrical and thermal device parameters, and its validity has been confirmed by using the thermal mapping analysis described in [2] on some test devices.

In this paper a validation of the proposed model has been done on a relatively high number of commercial Power MOS that have been electrically characterized to check whether the experimental detection of the relevant parameters accounted for in the analytical model leads to an accurate prediction of limitations in pulsed SOA at different pulse lengths.

II. THE THERMAL INSTABILITY CONDITION

The basic condition for thermal instability is given by

$$S = V_{DS}\alpha_T(I_D)Z_{TH}(t) \geq 1 \qquad (1)$$

where $\alpha_T(I_D)$ is the temperature coefficient of the Drain current and $Z_{TH}(t)$ is the thermal impedance at the time t. From the analysis reported in [3] it comes out that $\alpha_T(I_D)$ can be positive and its maximum is given by

$$\alpha_{TMAX} = \frac{\phi^2 K(T) T}{m} \qquad (2)$$

where K is the current factor in the SPICE level 1 MOS model, ϕ is the absolute value of the temperature coefficient of the threshold voltage V_{TH}, and m is the power mobility factor. By using this expression for α_{TMAX} and with reference to a power pulse of length t_P, (1) becomes [3]

$$\phi^2 K(T) \geq \frac{m}{V_{DS} Z_{TH}(t_P) T} \qquad (3)$$

where the condition has been expressed in terms of the purely electrical *figure of merit* $\phi^2 K(T)$. Thus, it is clear that the thermal instability is more likely to occur when the trasconductance g_{FS} is large and/or the absolute value of the threshold voltage temperature coefficient (TVTC) ϕ is high. When the value of $\phi^2 K(T)$ is large, a reduction of the Drain voltage V_{DS} is required in order to keep stable the device, which in turn might confine the theoretical SOA to voltages lower than the datasheet ratings.

From the above discussion, it follows that an accurate TVTC model illustrating its dependence of the basic technological parameters (i.e. channel doping, gate oxide, polysilicon doping) is of utmost importance for the design of Power MOSFETs. Unfortunately, all the TVTC models proposed in literature refer to conventional MOS transistors characterized by uniformly-doped channels, thus neglecting the complex underlying physics of nonuniform channels in Power double-diffused devices. Nevertheless, it has been numerically demonstrated that a generalized version [4] of a model proposed by Klaassen and Hes [5] can be favorably adopted in a large range of parameter values as a good compromise between complexity and accuracy. The formula is

$$\frac{\partial V_{TH}(T)}{\partial T} = \frac{\phi_{poly\_Si}(T)}{T} + \frac{3k}{q} + \frac{E_{G0}}{qT} + \left(2 + \frac{1}{C_{OX}}\sqrt{\frac{qN_{AP}\varepsilon_S}{\psi_B(T)}}\right)\left(\frac{\psi_B(T)}{T} - \frac{3k}{2q} - \frac{E_{G0}}{2qT}\right) \qquad (4)$$

being

$$\psi_B(T) = \frac{kT}{q}\ln\frac{N_{AP}}{n_i(T)}$$

and

$$\phi_{poly\_Si}(T) = \frac{kT}{q}\ln\left(\frac{n_i^2(T)}{N_{poly}\,N_{AP}}\right).$$

where N_{AP} represents the doping peak in the channel, E_{G0} is the extrapolated band-gap at 0 K, whilst all other terms have their customary meanings. In Fig.1

the calculated ϕ vs. N_{AP} is shown for various values of oxide thickness according to (4).

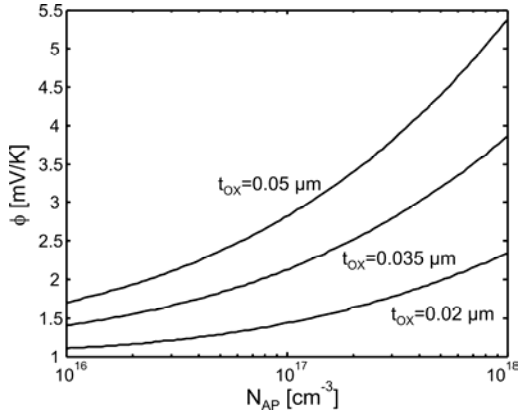

Fig.1. Calculated ϕ at $T = 300$ K as a function of channel doping peak for various gate oxide thicknesses.

Eq. (4) can be effectively adopted to evidence the relation between ϕ and the threshold voltage V_{TH}, whose value, contrarily to technological parameters, is easily accessible from datasheet. Fig.2 details the calculated behavior of ϕ vs. V_{TH} within the same parameter range of Fig.1.

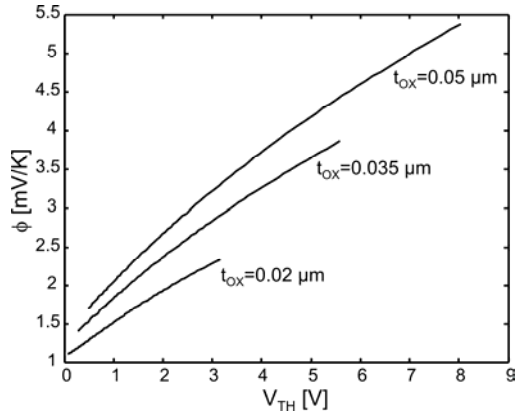

Fig.2. ϕ dependence on the threshold voltage V_{TH} for different gate oxide thicknesses evaluated via Eq. (4) at $T = 300$ K.

It can be observed that high ϕ values are associated to large threshold voltages, thus demonstrating that a high V_{TH} value might be regarded as an *undesirable symptom* of poor thermal ruggedness for the analyzed device, as will be experimentally evidenced in the following.

III. Device Characterization and Results

In order to validate the model described in Section II, we have chosen some Power MOS devices of two leading producers (indicated as A and B), with quite large values of trasconductance g_{FS} and threshold voltage V_{TH} spanning from values lower than 2 V (devices #A1 and #A2) to above 3 V (devices #A3, #A4, #B1, #B2, #B3). All the relevant parameter values obtained from datasheets are reported in Table 1. The devices have been electrically characterized through isothermal measurements (with pulse width of 50 μs). All the parameters playing a role in the model (i.e. K, V_{TH}, ϕ, m) have been extracted from the $\sqrt{I_D} - V_{GS}$ curves through the *quadratic extrapolation* approach, as reported in Fig.3. The measurements are made near 100°C because the instability onset is reached after the device is substantially heated above ambient temperature. The attained parameter values are listed in Table 2.

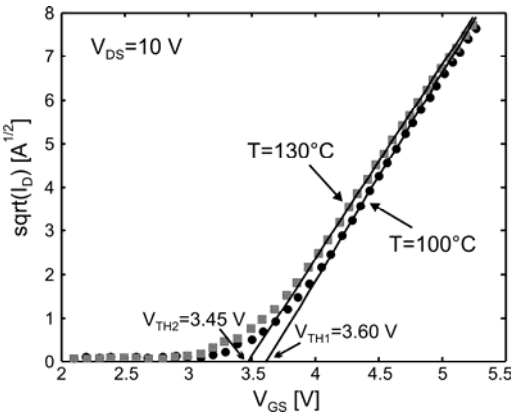

Fig.3. Transfer $\sqrt{I_D} - V_{GS}$ curve of #B3 in pulse operation at two temperatures: application of the quadratic extrapolation procedure.

From (3) we can define, for each power pulse condition (length t_P and Drain voltage V_{DS}), a set of curves delimitating the border between stability and instability in the plane (K, ϕ). Fig.4 shows the curves corresponding to three values of thermal impedance $Z_{TH}(t_P)$ at $V_{DS} = 55$ V (a Drain voltage near to that of "first breakdown" V_{DSS}) and $m = 1.5$. As can be seen, when the pulse length t_P is such as $Z_{TH}(t_P) = 0.5$ K/W, all the devices characterized by high threshold voltage values are located well over the stability limit, thus suggesting a possible thermal runaway at voltages *lower* than V_{DSS}, whereas the devices with low threshold voltage are unconditionally stable. Conversely, pulses leading to Z_{TH} values larger than 1 K/W make all the tested transistors lie in the thermally unstable region.

The proneness to thermal instability even in quite short pulse operation of devices with $V_{TH} > 3$ V has been demonstrated by recording the current during the pulsed bias condition. Let us consider the device #B1, which is characterized by the maximum thermal impedance $Z_{TH}(40\text{ ms}) = 1.0$ K/W (see Table 1) and the relatively low $\phi = 4.0\times10^{-3}$ V/K (see Table 2). #B1 has been biased for 40 ms by applying $V_{DS} = 15$ and 30 V and V_{GS} values such as to have the same initial power (90 W).

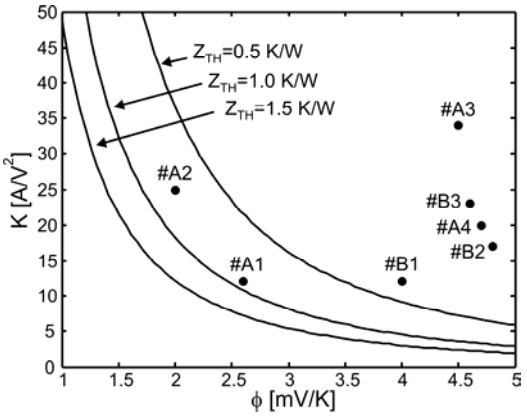

Fig.4. Stability plane for $V_{DS} = 55$ V . The device points refer to the actual values of ϕ , K from Table 2 for the different devices.

As can be seen in Fig.5, in both cases, the device shows a current increase with time indicating a positive α_T . However, the I_D evolution is different: a stable behavior is detected at $V_{DS} = 15$ V (Fig.5a), whereas a change in slope from downward to upward bending is observed at $V_{DS} = 30$ V (Fig.5b), as a clear evidence of the thermal instability onset [3]: the device fails shortly after this point due to localized thermal runaway.

Fig.6 shows the stability factor S for $\alpha_T = \alpha_{TMAX}$ as a function of the power pulse length t_P at $V_{DS} = 30$ (6a) and 15 V (6b) for all the tested devices. Let us consider the $V_{DS} = 30$ V case. As can be seen, when the pulse is shorter than 1 ms, all the transistors are unconditionally stable. On the other hand, for $t_P > 2$ ms the device #B3 moves to the thermal instability region. For $t_P = 40$ ms (indicated by the vertical dashed line) only the devices #A1 and #A2 (characterized by low threshold voltage values) are still stable.

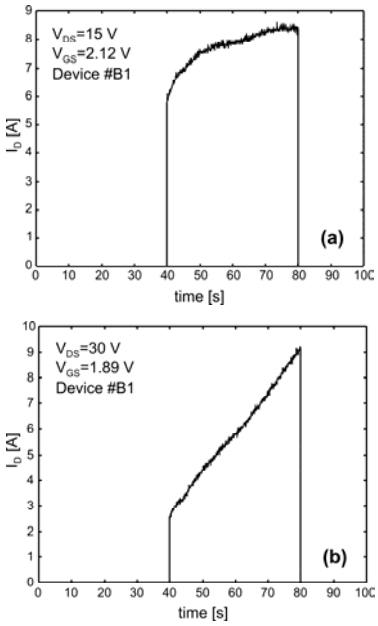

Fig.5. Current plots of device #B1 for the same initial power bias of 90 W and pulse duration of 40 ms: $V_{DS} = 15$ V (a); $V_{DS} = 30$ V (b).

The device #B1, in particular, exhibits a factor $S = 1.5$ (black dot), as a further evidence of the behavior depicted in Fig.5b. Note that #A1 and #A2 are well below the "critical" border curve even at $t_P = 100$ ms , although their thermal resistances are higher than those of the other transistors (with the exception of #B1). This behavior seems to confirm that a high V_{TH} value may represent a qualitative indicator of low thermal ruggedness. In the case $V_{DS} = 15$ V it can be seen that, with the exception of the transistor #B3 (which is characterized by high values of both ϕ and Z_{TH}), the stability factor of all the devices remains confined below unity for a pulse length up to 40 ms.

Table 1. Datasheet parameter values.

Device	V_{DSS} (V)	I_{DMAX} (A)	V_{TH} (V)	g_{FS} @ V_{DS} I_D (S)	Z_{TH}@ 40 ms (K/W)
#A1	60	38	1 – 2.5	24 @ 15 V 19 A	1.15
#A2	60	55	1 - 2	30 @ 15 V 27 A	1.0
#A3	55	80	2 - 4	40 @ 15 V 18 A	0.3
#A4	60	60	2 - 4	35 @ 15 V 30 A	0.4
#B1	55	64	2 - 4	22 @ 25 V 32 A	1.0
#B2	55	110	2 - 4	42 @ 25 V 59 A	0.62
#B3	55	110	2 - 4	44 @ 25 V 59 A	0.75

Table 2. Electrical device parameters extracted through pulsed $I_D - V_{GS}$ measurements near 100°C.

Device	K (A/V^2)	V_{TH} (V)	ϕ (mV/K)	m	α_{TMAX} (A/K)
#A1	12	1.73	2.6	1.6	0.017
#A2	25	1.77	2.0	1.5	0.027
#A3	34	4.77	4.5	1.2	0.19
#A4	20	3.33	4.7	1.6	0.10
#B1	12	3.16	4.0	1.5	0.05
#B2	17	3.40	4.8	1.5	0.11
#B3	23	3.60	4.6	1.5	0.12

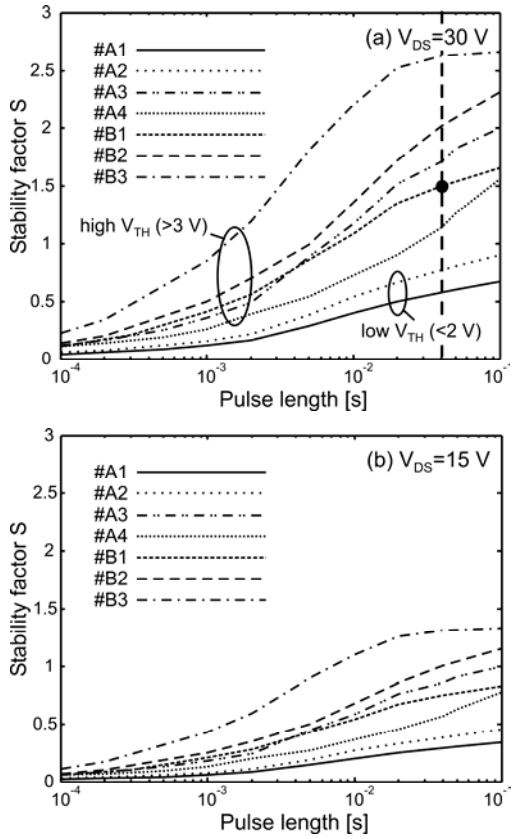

Fig.6. Stability plane for the tested devices as a function of the power pulse duration for $V_{DS} = 30$ V (a); $V_{DS} = 15$ V (b).

Lastly, a radiometric analysis [2] of the device #A3 under 20 ms-long pulse operation has been performed at $V_{DS} = 20$ V and V_{GS} such as $I_D = 29$ A at room temperature. Fig.7a details the temperature behavior vs. time of the hottest point (located in the innermost region) and a side point 1.7 mm far from the center. Both temperatures increase as a consequence of the positive α_T. However, after 17-18 ms, the hottest point tends to thermal instability; indeed at this time instant it happens that $\alpha_T = \alpha_{TMAX}$ ($I_D = 68$ A) and the stability factor S goes beyond unity (see insert in Fig.7a). Further experimental evidence for the proposed model is therefore attained. In Fig.7b the overall temperature map at the end of the applied pulse is illustrated: the hot-spot occurrence due to the condition $S > 1$ reached by the elementary devices located over the central region is apparent.

IV. Conclusions

A simple analytical model for the electrothermal instability occurrence in Power MOS transistors has been experimentally verified on a number of commercially available devices and its capability to predict limitations in the theoretical pulsed SOA on the basis of a few easily measurable parameters has been demonstrated. In particular, the critical role played by the temperature coefficient ϕ has been enlightened and an accurate expression illustrating its dependence on all relevant technological parameters has been presented. It has been shown that devices with high threshold voltage values may suffer from low thermal ruggedness, even when characterized by not large thermal impedances. Owing to the encouraging experimental support, the formulations proposed can be effectively adopted at the design stage in order to provide possible countermeasures to minimize thermally-induced limitations in pulsed SOA without worsening the electrical device features.

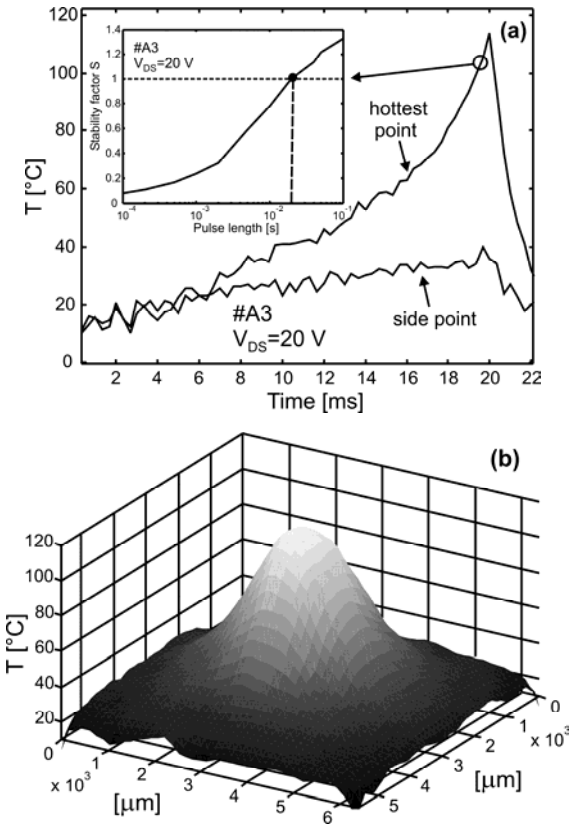

Fig.7. Radiometric temperature detection for the device #A3 operated under pulsed bias conditions: thermal behavior of the hottest point and of a side point vs. time (a); overall temperature map at the end of the applied pulse (b).

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